Data Sheet

Version: 2.5

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LTC Play-Speed Reader Chip

LTC-PSR

Alpermann+Velte

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A1 Copyright

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Features

- CMOS process technology for low power consumption
- Operating temperature range of 0 to 70 °C
- 8-bit bi-directional databus with high impedance tristate drivers
- Accepts time code at the normal play speed, forward and reverse
- SMPTE/EBU longitudinal time code input, 8-bit parallel and serial output
- Four user selectable interrupt modes
- Output of a direction flag
- Output of the time code bit clock and data
- Output of a synchronword flag
- Edge sensitive interrupt input (CTL)
- Time data and user group data are simultaneously accessible

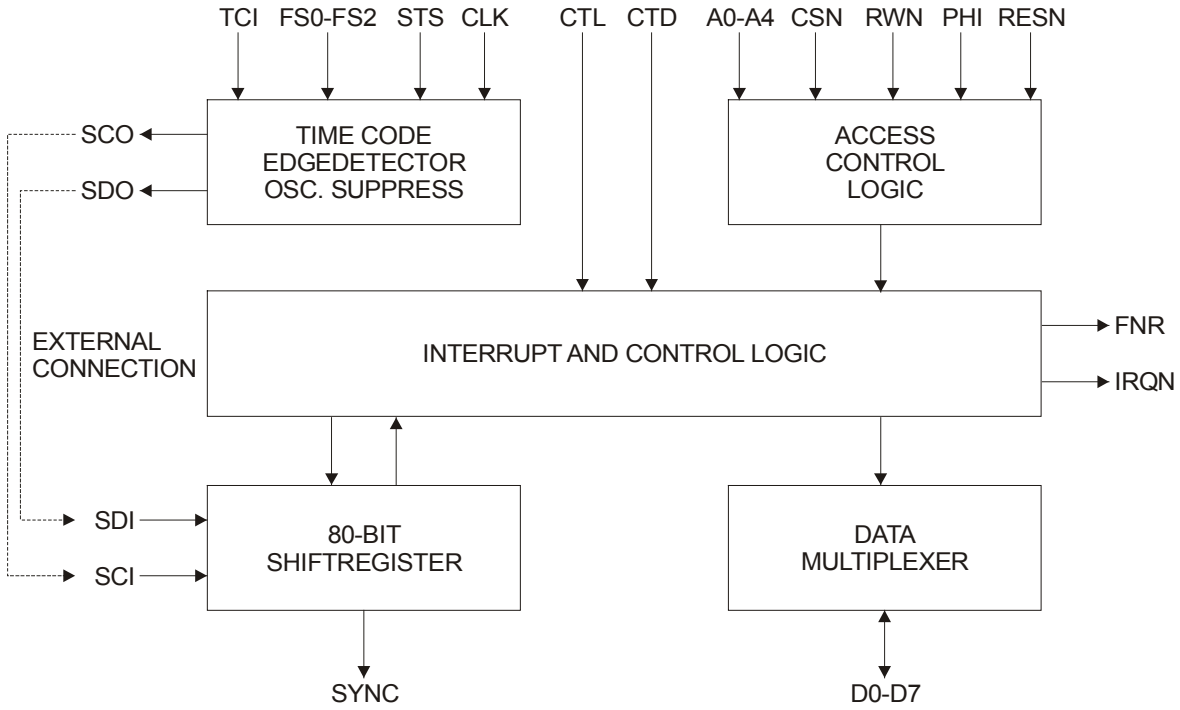
General Description

The LTC-PSR is a FPGA in a 44 pin PLCC package and designed to read the SMPTE/EBU time and control code of the longitudinal format, or – according to ANSI/SMPTE 12M-1995 – linear format (LTC).

The LTC-PSR is designed to communicate with a microprocessor. All time data (26 bits), user data (32 bits) and status data (6 bits) of the 80-bits time code word are simultaneously accessible.

The LTC-PSR works with digital inputs and outputs. Oscillations (up to 4 CLK cycles) on the edges of the digital time code input are suppressed internal. The accepted LTC input frequency range depends on the system clock and the selection at pins FS0-FS2 and STS. The accepted range is 19.2-38.2 frames per second (STS=H) and 16.0-31.9 frames per second (STS=L) if the system clock has one of the proposed value together with the appropriate setting of FS0-FS2 (see signal description). The range at STS=H covers the LTC formats of 24, 25 or 30 frames per second at normal speed. Using other system clock frequencies the range will be linearly shifted, e.g. using 16 MHz instead of 8 MHz (STS=H) results in 38.4-76.4 frames per second.

Block Diagram



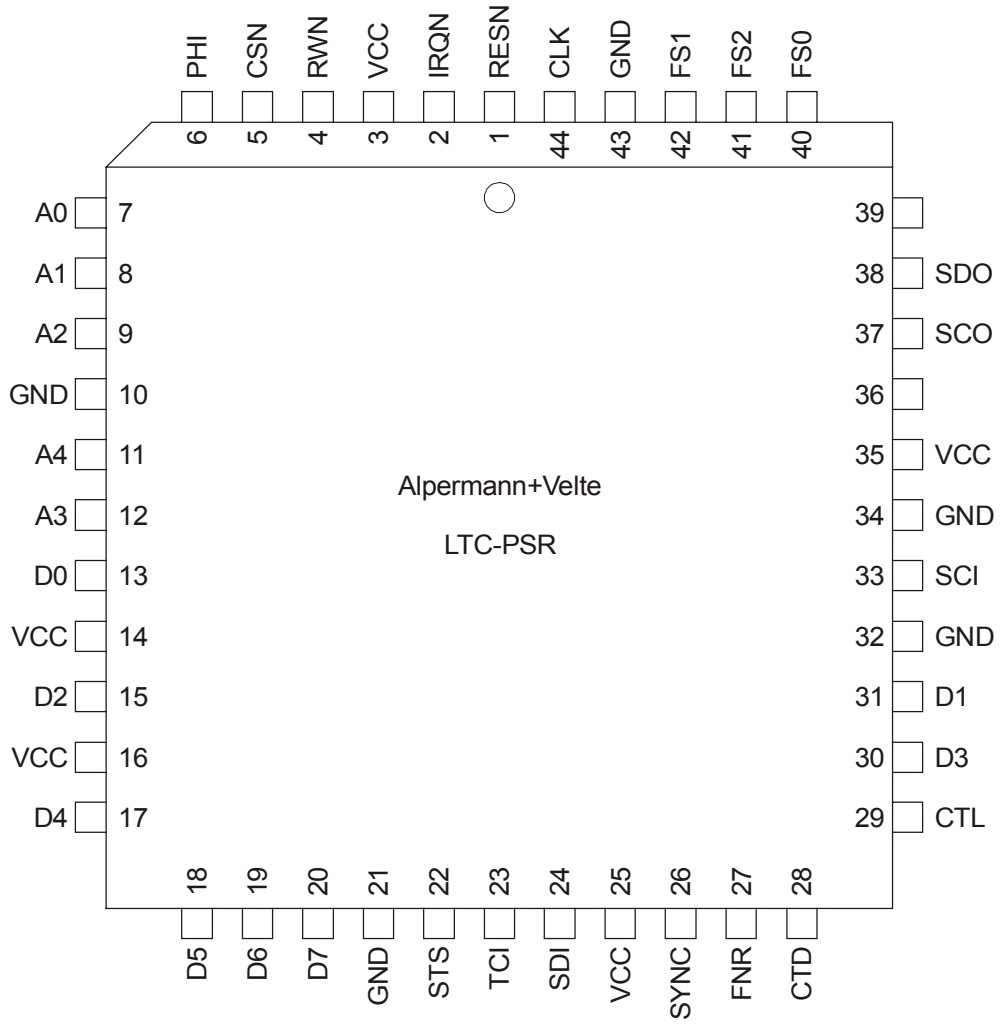
Pin Function Table

Pin No.	Pin Name	I/O	Description
1	RESN	I	System reset
2	IRQN	OD[1]	Interrupt request
3	VCC	I	Power supply
4	RWN	I	Read/Write control
5	CSN	I	Chip select
6	PHI	I	CPU bus control
7	A0	I	Register address
8	A1	I	Register address
9	A2	I	Register address
10	GND	I	Logic ground
11	A4	I	Register address
12	A3	I	Register address
13	D0	I/O	Data bus
14	VCC	I	Power supply
15	D2	I/O	Data bus
16	VCC	I	Power supply
17	D4	I/O	Data bus
18	D5	I/O	Data bus
19	D6	I/O	Data bus
20	D7	I/O	Data bus
21	GND	I	Logic ground
22	STS	I	Standard select
23	TCI	I	Timecode input
24	SDI	I	Serial data in, connect to SIO
25	VCC	I	Power supply
26	SYNC	O	Synchron word flag
27	FNR	O	Direction
28	CTD	I	Readable userbit (CTL direction)
29	CTL	I	Input for hardware interrupt (CTL pulse)
30	D3	I/O	Data bus
31	D1	I/O	Data bus
32	GND	I	Logic ground
33	SCI	I	Serial clock in, connect to SCO
34	GND	I	Logic ground
35	VCC	I	Power supply
36		O	(unassigned)
37	SCO	O	Serial clock out, connect to SCI
38	SDO	O	Serial data out, connect to SII
39		O	(unassigned)
40	FS0	I	CLK frequency select
41	FS2	I	CLK frequency select
42	FS1	I	CLK frequency select
43	GND	I	Logic ground
44	CLK	I	System clock, select with FS2..FS0

All unassigned pins are defined as outputs and have to be left open.

[1] *OD = Open Drain*

Pin Diagram



All unassigned pins are defined as outputs and have to be left open.

Signal Description

Pin Name	Description
TCI	Time code in. Input of the digitalized LTC signal.
CLK	System clock. Possible frequencies are 1, 2, 4, 6, 8 or 10 MHz, selectable by FS0-FS2.
FS0-FS2	CLK frequency select. Please refer to the following table: CLK (MHz) 1 2 4 6 8 10 FS0 L H L H L H FS1 L L H H L L FS2 L L L L H H
STS	Standard select. STS = H: 30 frames per second (-34%, +27%) STS = L: 25 frames per second (-34%, +27%)
SCO	Serial clock out. Connect to SCI for normal operation. The rising edge is used to shift out decoded time code data at pin SDO.
SDO	Serial data out. Connect to SDI for normal operation.
SCI	Serial clock in. Connect to SCO for normal operation.
SDI	Serial data in. Connect to SDO for normal operation.
SYNC	A positive pulse (pulse width = width of a time code bit) is generated each time the synchronizing word is detected within the time code.
FNR	Output of a direction flag, derived from the synchronizing word of the time code. FNR = L: forward direction FNR = H: backward direction Please note that this flag is only significant if simultaneously the SYNC-pulse has occurred.
IRQN	The interrupt request output signal is generated (logical 0) whenever an interrupt flag bit and the corresponding enable bit set. The time code reader control logic and/or the CTL input may cause an interrupt signal. The interrupt modes of the reader are programmable. The output is an open-drain configuration, it needs a external pull-up resistor allowing to wired-ANDed to a common microprocessor IRQ input.
D0-D7	Data bus D0-D7 are in high impedance state if CSN = H D0-D7 are used as data in- or outputs if CSN = L
A0-A4	Address bus. This input selects the required internal registers.
CSN	Chip select CSN = H: chip is deselected CSN = L: chip is selected

Pin Name	Description
RWN	Read/Write. Controls the direction of the internal data bus buffers RWN = L : CPU → LTC-PSR (Write) RWN = H : LTC-PSR → CPU (Read)
PHI	PHI controls the storing of data into the internal registers and the data bus drivers. For read cycles (CSN = L and RWN = H) the data bus drivers are active while PHI = H. For write cycles (CSN = L and RWN = L) storage is done by the negative edge of PHI, the positive edge of CSN or the positive edge of RWN, depending of which edge comes first. For some microprocessors PHI is the bus clock (65xx: PHI2, 68xx: E), other needs a simple interface logic (see applications).
RESN	Reset. L clears all internal registers.
CTL	Hardware interrupt. This input signal may come from an external hardware. A rising edge at this input sets an internal flag (CTL-FF) and forces the IRQN output to low level if the corresponding enable bit is set. Typically track pulses of an audio or video recorder is used as input.
CTD	User bit. This input signal may come from an external hardware. The CPU may read the state of this input pin by access of an internal register. Typically a CTL-pulse direction flag is used as input.

Internal Registers

A complete time code word contains 80 bits. There are 26 bits of time data, 32 bits of user data, 16 bits of sync word and 6 bits of status data.

Except the 16 bit of the sync word all bits are accessible and may be read out on the databus of LTC-PSR.

The following table shows how to select the data and gives a short description of the bits.

Dec	Hex	A4-A0	R/W	D0-D7	LTC Bit No.	Description
0	00	0 0 0 0 0	R	D0 D1 D2 D3	0 1 2 3	Units of Frames
				D4 D5 D6 D7	4 5 6 7	Binary Group 1
1	01	0 0 0 0 1	R	D0 D1	8 9	Tens of frames
				D2 D3	10 11	Drop Frame Flag Color Frame Flag
				D4 D5 D6 D7	12 13 14 15	Binary Group 2
2	02	0 0 0 1 0	R	D0 D1 D2 D3	16 17 18 19	Units of Seconds
				D4 D5 D6 D7	20 21 22 23	Binary Group 3

Dec	Hex	A4-A0	R/W	D0-D7	LTC Bit No.	Description
3	03	0 0 0 1 1	R	D0	24	Tens of Seconds
				D1	25	
				D2	26	
				D3	27	Status Bit 27[1]
				D4	28	Binary Group 4
				D5	29	
				D6	30	
				D7	31	
4	04	0 0 1 0 0	R	D0	32	Units of Minutes
				D1	33	
				D2	34	
				D3	35	
				D4	36	Binary Group 5
				D5	37	
				D6	38	
				D7	39	
5	05	0 0 1 0 1	R	D0	40	Tens of Minutes
				D1	41	
				D2	42	
				D3	43	Status Bit 43[2]
				D4	44	Binary Group 6
				D5	45	
				D6	46	
				D7	47	
6	06	0 0 1 1 0	R	D0	48	Units of Hours
				D1	49	
				D2	50	
				D3	51	
				D4	52	Binary Group 7
				D5	53	
				D6	54	
				D7	55	

[1] *Status Bit 27: 30- and 24-frame: Polarity correction, 25-frame: Binary Group Flag 0 (BGF0)*

[2] *Status Bit 43: 30- and 24-frame: Binary Group Flag 0 (BGF0), 25-frame: Binary Group Flag 2 (BGF2)*

Dec	Hex	A4-A0	R/W	D0-D7	LTC Bit No.	Description
7	07	0 0 1 1 1	R	D0 D1	56 57	Tens of Hours
				D2	58	Status Bit 58[1]
				D3	59	Status Bit 59[2]
				D4 D5 D6 D7	52 53 54 55	Binary Group 7
15	0F	0 1 1 1 1	R	D7		Direction bit FNR, L = forward
24	18	1 1 0 0 0	R/W	D0 D1 D2 D3		TCIE BITA BITB CTEN
			R	D4 D5 D6 D7		CTD CTL-FF TCI-FF 80-bit Flag
30	1E	1 1 1 1 0	W			TCI-FF reset
31	1F	1 1 1 1 1	W			CTL-FF reset

[1] *Status Bit 58: Binary Group Flag 1 (BGF1)*

[2] *Status Bit 59: 30- and 24-frame: Binary Group Flag 2 (BGF2), 25-frame: Polarity correction*

Programmable Interrupt Mode

The decoded SMPTE/EBU timecode (SIO) is clocked with the SCO-signal into an internal 80-bit shift register (SR). The user may choose between four interrupt modes to define at what time the data in the SR are acceptable.

If any interrupt condition is met, the IRQN output switches from high impedance to L-level. To preset the interrupt conditions, the user has to set 4 control bits. This will be done by a simple write operation to the following register.

Dec	R/W	D7	D6	D5	D4	D3	D2	D1	D0
24	W	Not used				CTEN	BITB	BITA	TCIE

Interrupt-signal IRQN disabled	0	X	X	0
IRQN from CTL input enabled	1	X	X	X
IRQN if a synchronizing word *and* 80 bits have been clocked	X	0	0	1
IRQN if only the synchronizing word has been detected	X	0	1	1
IRQN if only 80 bits have been clocked	X	1	0	1
IRQN if a synchronizing word *or* 80 bits have been clocked	X	1	1	1

Independent of the status of CTEN or TCIE every interrupt condition of CTL (rising edge) and time code reader (as defined by BITA and BITB) is indicated by two internal flip-flops: CTL-FF and TCI-FF. The CTEN and TCIE only switch the access to IRQN output. The state of the flip-flops is represented in register 24:

Dec	R/W	D7	D6	D5	D4	D3	D2	D1	D0
24	R	80-bit Flag	TCI-FF	CTL-FF	CTD	CTEN	BITB	BITA	TCIE

Reading out the corresponding bits makes it possible to decide whether an interrupt has occurred or not. Once a flip-flop is set it has to be resetted by a simple write operation:

Dec	Hex	A4-A0	R/W	D0-D7	Description
30	1E	1 1 1 1 0	W	Don't care	TCI-FF reset
31	1F	1 1 1 1 1	W	Don't care	CTL-FF reset

Electrical Characteristics

5.0V Operating Conditions

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	-0.5 to +7.0	Volts
V_I	Input Voltage	-0.5 to V_{CC} + 0.5	Volts
V_O	Output Voltage	-0.5 to V_{CC} + 0.5	Volts
T_{STG}	Storage Temperature	-65 to +150	°C

Recommended Operating Conditions

Parameter	Min.	Max.	Units
Temperature Range[2]	0	+70	°C
Power Supply V_{CC}	4.75	5.25	V

Electrical Specifications

Symbol	Parameter	Min.	Max.	Units
V_{OH}[3]	(I_{OH} = -10mA)[4]	2.4		V
	(I_{OH} = -6mA)	3.84		V
V_{OL}[3]	(I_{OL} = 10mA)[4]		0.5	V
	(I_{OL} = 6mA)		0.33	V
V_{IL}		-0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[4]			500	ns
C_{IO} I/O Capacitance[4, 5]			10	pF
Standby Current, I_{CC}[6]			3	mA
Leakage Current[7]		-10	10	µA

[1] *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommend Operating Conditions.*
[2] *Ambient temperature (T_A).*
[3] *Only one output tested at a time. V_{CC} = min.*
[4] *Not tested, for information only.*
[5] *V_{OUT} = 0V, f = 1MHz.*
[6] *Typical standby current = 1mA. All outputs unloaded. All inputs = V_{CC} or GND.*
[7] *V_O, V_{IN} = V_{CC} or GND.*

3.3V Operating Conditions

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	-0.5 to +7.0	Volts
V_I	Input Voltage	-0.5 to V_{CC} + 0.5	Volts
V_O	Output Voltage	-0.5 to V_{CC} + 0.5	Volts
I_{IO}	I/O Sink/Source Current[2]	±20	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Recommended Operating Conditions

Parameter	Min.	Max.	Units
Temperature Range[3]	0	+70	°C
Power Supply V_{CC}	3.0	3.6	V

Electrical Specifications

Symbol	Parameter	Min.	Max.	Units
V_{OH}[4]	(I_{OH} = -4mA)[5]	2.15		V
	(I_{OH} = -3.2mA)	2.4		V
V_{OL}[4]	(I_{OL} = 6mA)		0.4	V
V_{IL}		-0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[5]			500	ns
C_{IO} I/O Capacitance[5, 6]			10	pF
Standby Current, I_{CC}[7]			3	mA
Leakage Current[8]		-10	10	µA

[1] *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommend Operating Conditions.*

[2] *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND -0.5V, the internal protection diode will be forwarded biased and can draw excessive current.*

[3] *Ambient temperature (T_A).*

[4] *Only one output tested at a time. V_{CC} = min.*

[5] *Not tested, for information only.*

[6] *V_{OUT} = 0V, f = 1MHz.*

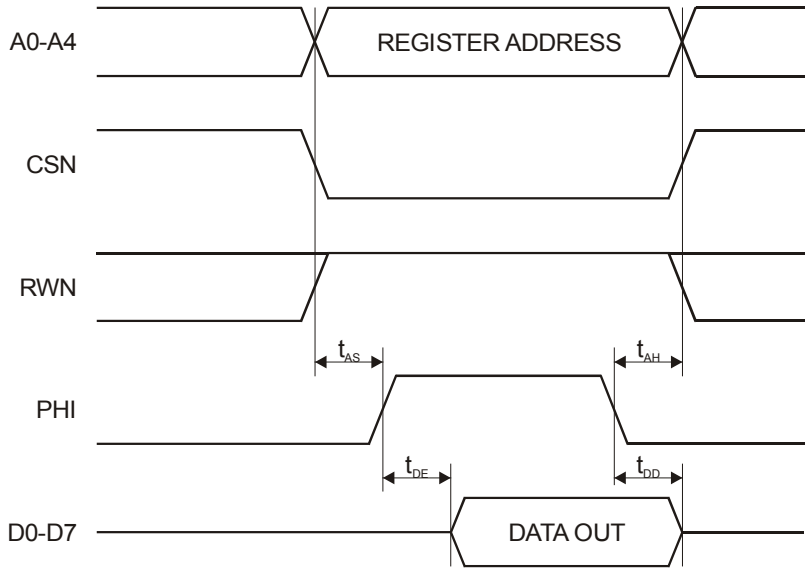
[7] *Typical standby current = 1mA. All outputs unloaded. All inputs = V_{CC} or GND.*

[8] *V_O, V_{IN} = V_{CC} or GND.*

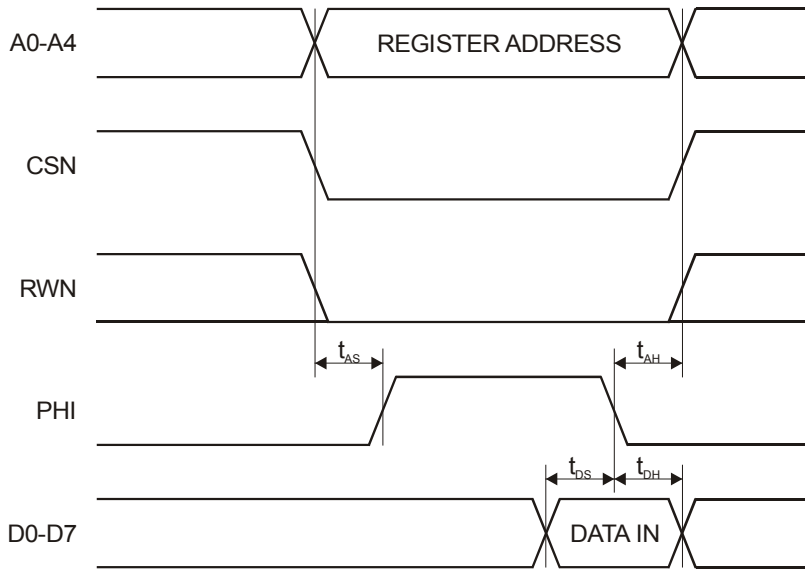
Switching Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AH}	Address Bus Hold Time	0			ns
t_{AS}	Address Bus Setup Time	0			ns
t_{DD}	Data Bus Disable Time			50	ns
t_{DE}	Data Bus Enable Time			50	ns
t_{DH}	Data Bus Hold Time	50			ns
t_{DS}	Data Bus Setup Time	50			ns

Read Timing



Write Timing



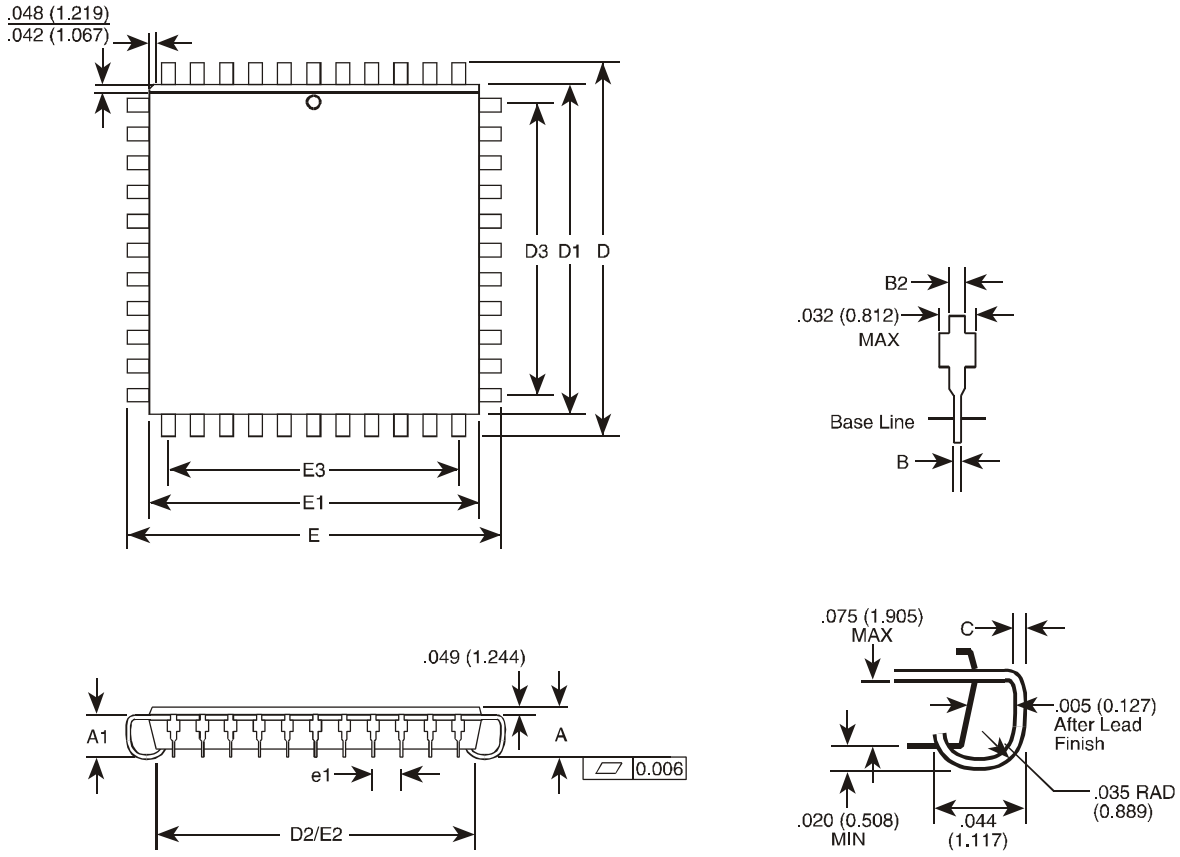
Physical Dimensions

Plastic Leaded Chip Carrier Package, 44 pins (PLCC 44)

JEDEC Equivalent: MS007 AB VAR

Symbol	Min.	Max.
A	0.155 (3.937)	0.175 (4.445)
A1	0.090 (2.286)	0.130 (3.302)
B	0.013 (0.330)	0.027 (0.686)
B2	0.026 (0.660)	0.032 (0.813)
C	0.007 (0.178)	0.013 (0.330)
D/E	0.670 (17.02)	0.710 (18.03)
D1/E1	0.640 (16.26)	0.660 (16.76)
D2/E2	0.590 (14.99)	0.630 (16.00)
D3/E3	0.50 (12.70) nominal	
e1	0.050 (1.270) BSC[1]	

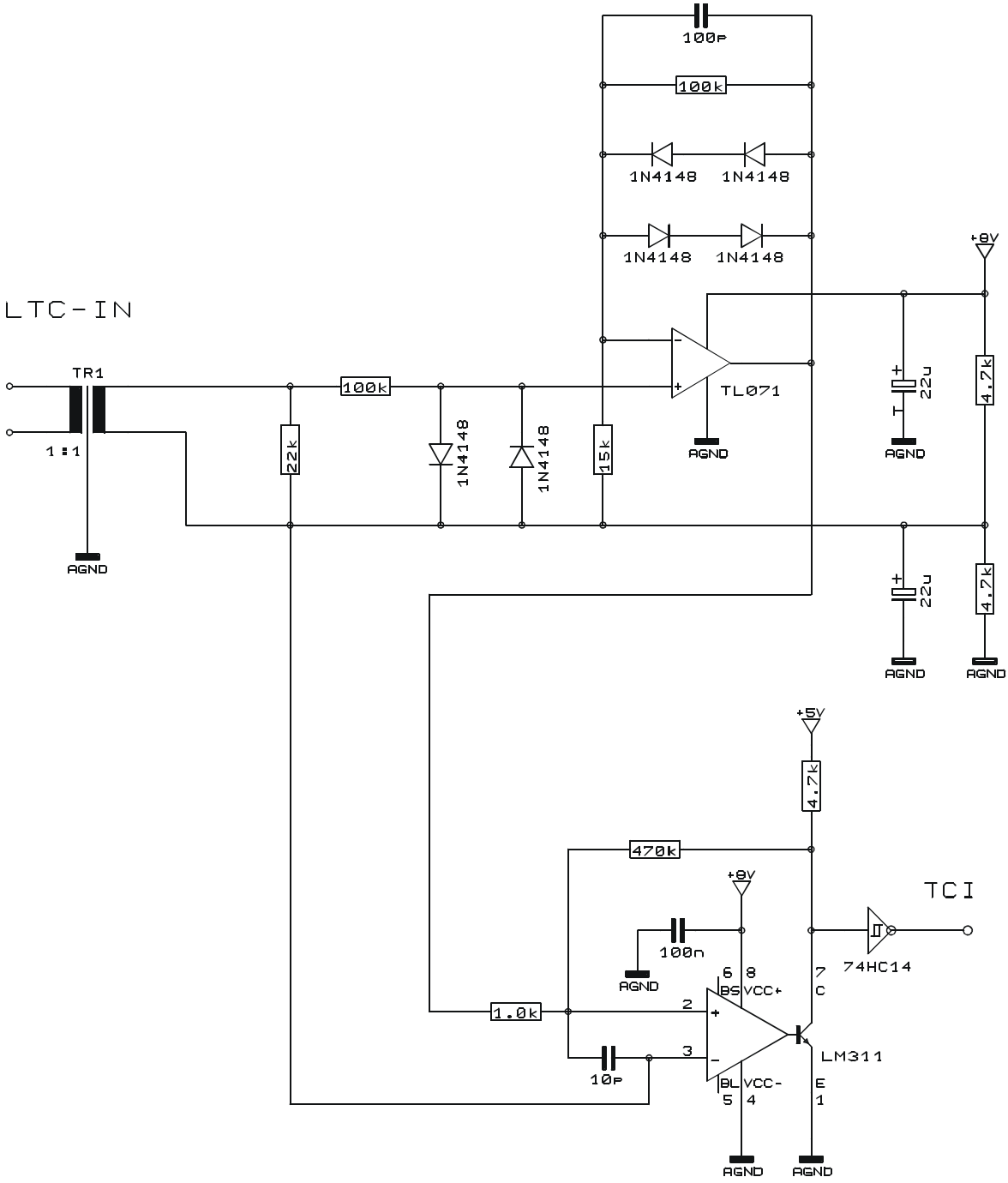
All dimensions are in inches (millimeters).



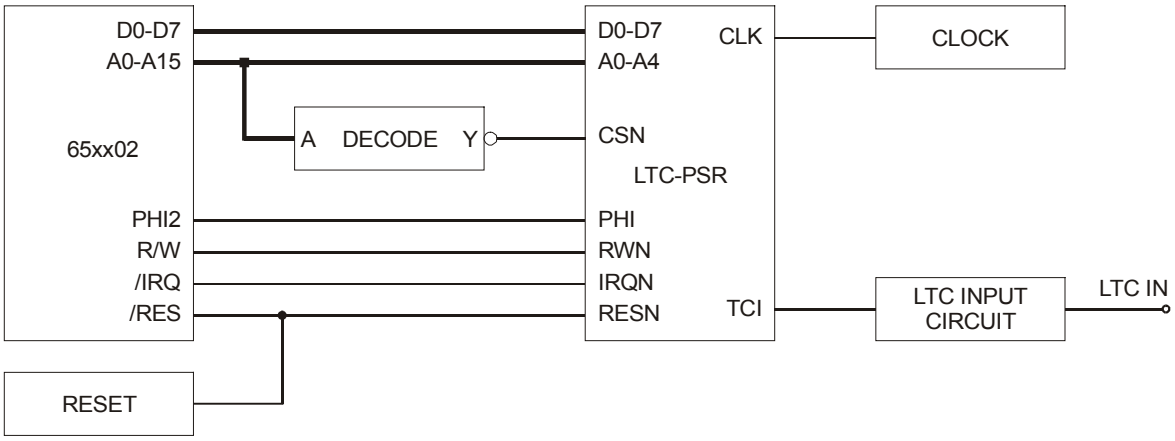
[1] *BSC – Basic Space between Centers*

Applications

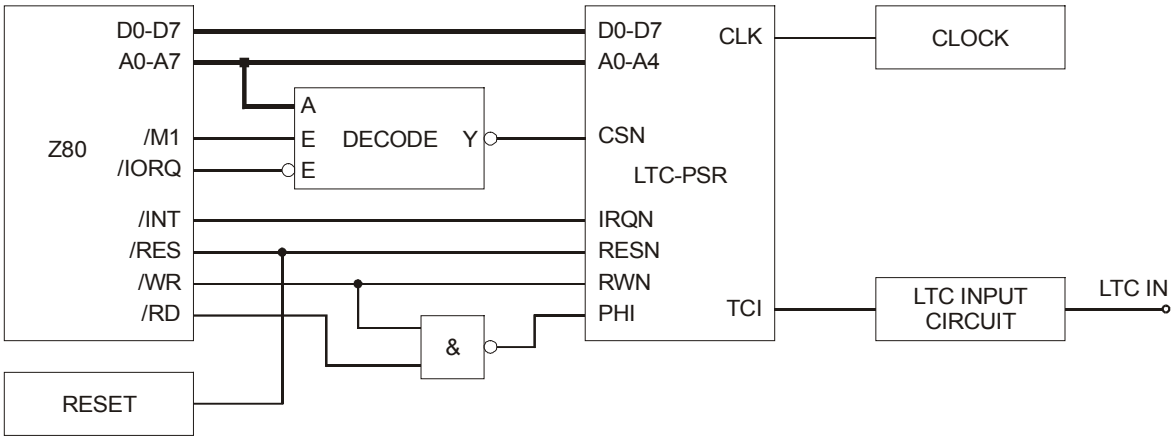
LTC-Signal Input Circuit



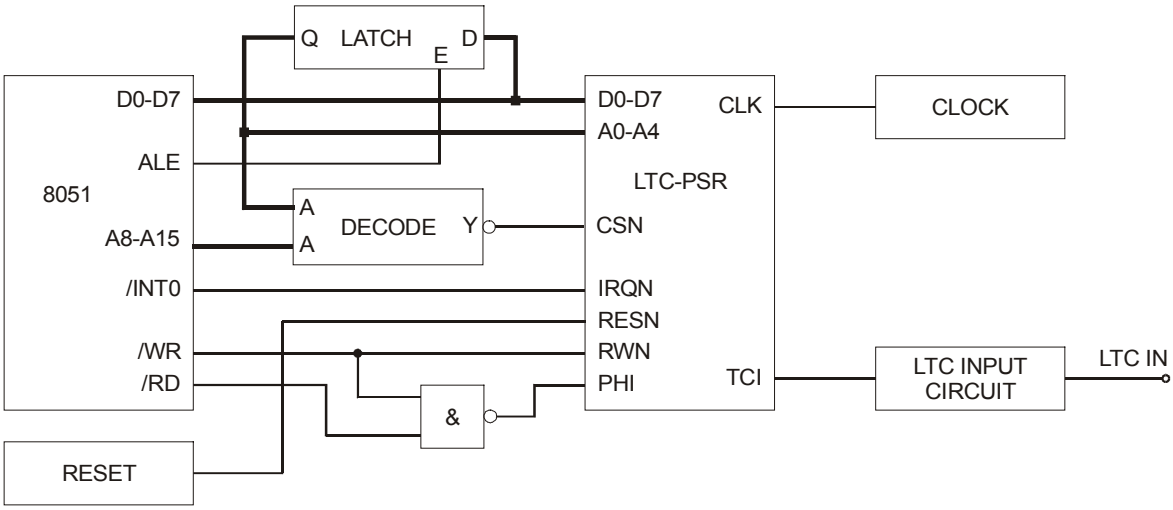
Interface to 65xx02 CPU



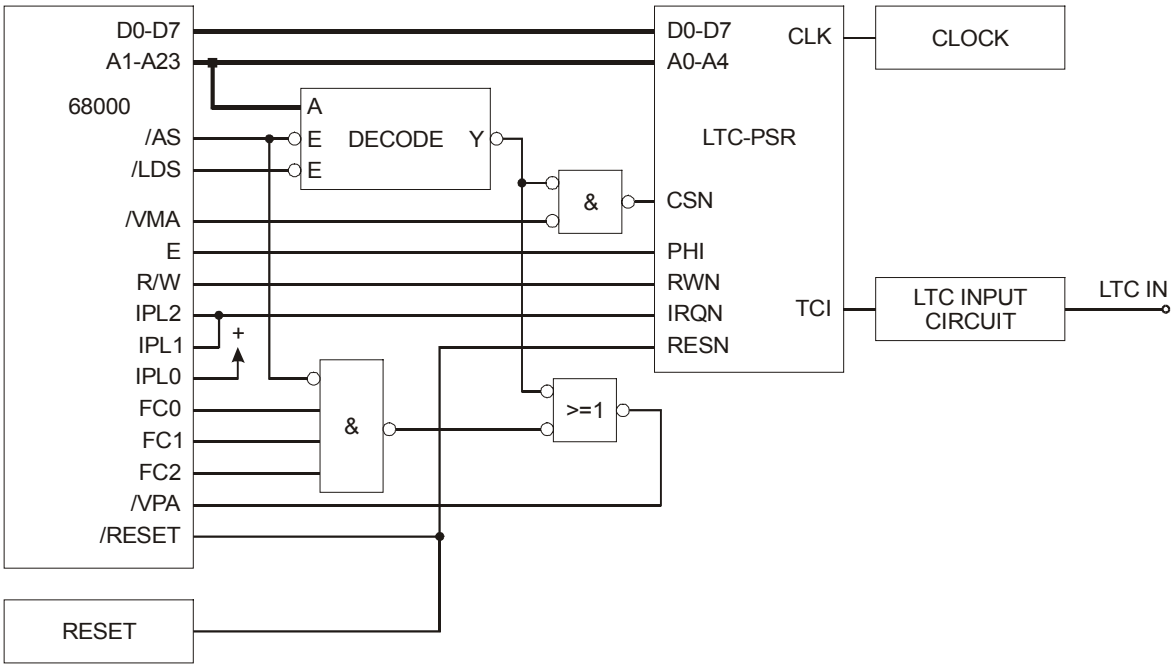
Interface to Z80 CPU



Interface to 8051 CPU



Interface to 68000 CPU[1]



[1] *Synchronous Mode, Interrupt Level 6 used, Autovector used*