

D-VITC Reader and Generator Chip

AV-DVITC

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For further information, contact your local dealer or

Alpermann+Velte

Electronic Engineering GmbH
D-42369 Wuppertal, Otto-Hahn-Str. 42
Fon.: ++49 - (0)202 – 244 111 0
Fax: ++49 - (0)202 – 244 111 5
E-Mail: info@alpermann-velte.com
Internet: <http://www.alpermann-velte.com>

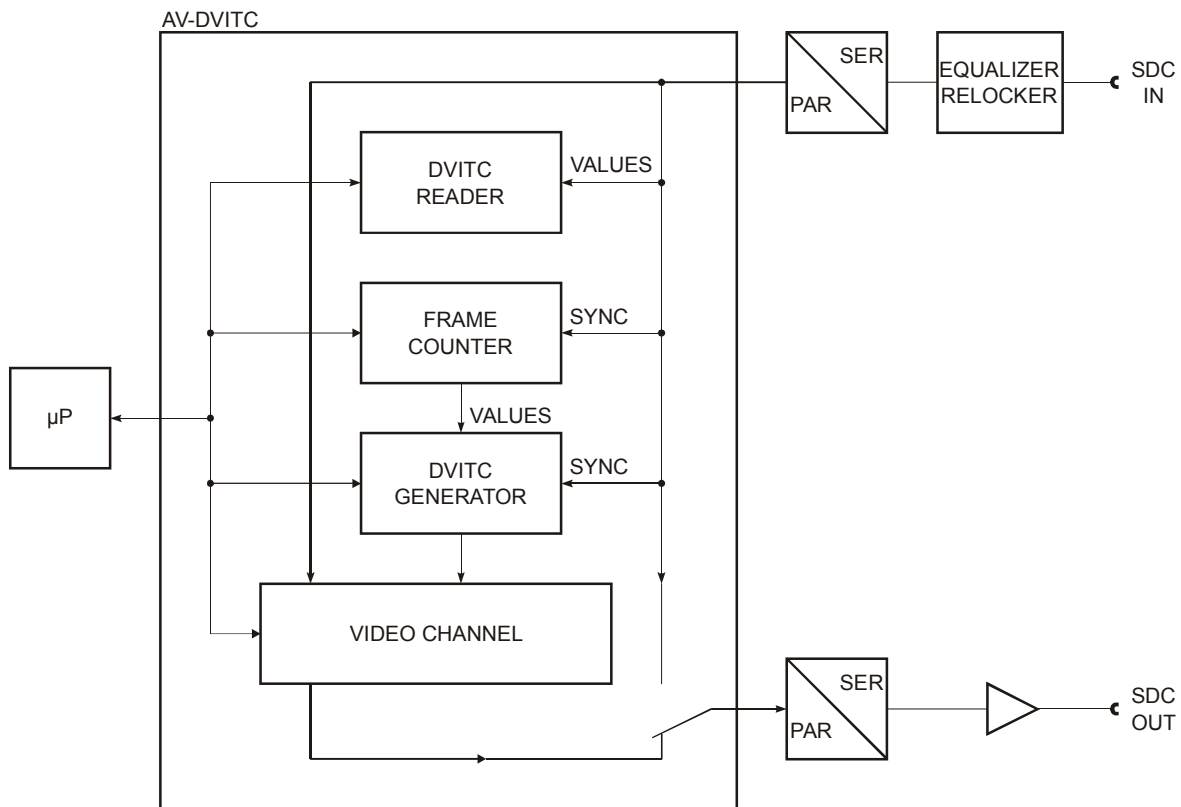
Features

- ANSI/SMPTE 266M-1994 compatible D-VITC reader and generator in one device
- ITU-R-601 compatible 10- or 8-bit, 27 MHz, 4:2:2 parallel video channel
- Pass-through and short-circuit modes to bypass D-VITC generation
- 8-bit parallel interface, multiplexed or non-multiplexed data and address bus, direct compatible to popular microprocessors like 8051, 80x86, Z80, etc.
- D-VITC time, user group and status data simultaneously accessible
- Independent interrupt sources from D-VITC reader and generator, V-, V1- and V2-pulse
- Stand-alone frame counter for free-running D-VITC generation in 25- or 30-frame, drop or non-drop mode
- CMOS process technology for low power consumption
- Single 5 volt power supply
- 84-pin PLCC package
- Temperature range 0 to 70 °C

General Description

The AV-DVITC is a FPGA in a 84 pin PLCC package and designed to read and generate the ANSI/SMPTE 266M D-VITC time and control code. All time data (26 bits), user data (32 bits) and status data (6 bits) of the 90-bits time code word are simultaneously accessible. The generator has an optional frame counter for stand-alone free-running D-VITC generation.

Block Diagram



Functions

Video Channel

Digital video is accepted in parallel format at 27 MHz. Input data is connected to DVI9:0 and clocked by DVIC signal, the video input clock, that synchronizes all processing of the video data stream internally. The video stream passes several internal stages. Sync pulses (H, V, F) and D-VITC reader data are extracted and D-VITC generator data is inserted. The finished video signal is output in parallel format again. The parallel data DVO9:0 are clocked to the next chip with the DVOC signal. It is possible to switch off the clock output to disable output of digital video. The exact number of internal stages in normal operating mode is six, so at 27 MHz the output video is delayed relative to the input by 222 ns.

The internal stages can be bypassed in two ways. The pass-through mode inhibits any modification but the video passes all internal stages. So, the delay of the video is the same as in normal operation mode. In opposite to that the short-circuit mode bypasses almost any stage, so the delay of the video is minimized. Switching from normal operation mode to pass-through mode is done without any timing errors in the video stream, but switching to short-circuit mode produced a short disturbance because some video samples are lost.

The video channel is programmable to 8- or 10-bit operation. In 8-bit mode DVI1 and DVI0 inputs are ignored and DVO1 and DVO0 output are forced to L-level.

All inputs and outputs are TTL compatible. AV-DVITC is designed to connect directly to GENLIX™ products family of Gennum Corporation. For details see <http://www.gennum.com>.

D-VITC Reader

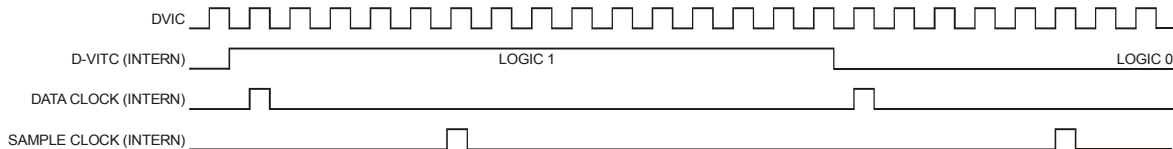
D-VITC is extracted from the video source by comparing the luminance samples (Y) with a programmable threshold. This threshold has to be set to half the peak level of the D-VITC in 8-bit notation. If the D-VITC in the video source was generated from a D-VITC generator, the optimal threshold level is 68_{16} , however if the video source contains a digitalized analogue VITC it might be necessary to adapt the threshold dynamically by software.

For special purposes the D-VITC reader can be programmed to get its data from an external source. With this pin it is possible to read the time code data from an other video channel, even reading of a analogue VITC is possible.

D-VITC will be read from selected lines. The line selection is programmable by internal registers. One or two lines, a block of lines or all lines of the vertical interval are selectable. A block of lines is used if the position of the D-VITC is unknown or changing. After reading the first correct D-VITC an interrupt flag will be set and an interrupt will occur if the corresponding interrupt enable bit is set. The interrupt flag has to be cleared before a new D-VITC can be read.

In the selected line reading will start with the first positive edge of the D-VITC input signal. This triggers two settable timers. The first timer specifies the length of a VITC bit. The other timer supplies a sample pulse to latch the VITC bit level (H or

L). Again, if the D-VITC was generated by a D-VITC generator, the bit timing is fixed, however if the source is a digitalized analogue VITC signal, the timing might be variable. To calculate the bit length set value, the length of a VITC bit (standard 555 ns) is divided by the period time of the digital video input clock (DVIC) reduced by 1. Set value of the sample pulse should be max. half of the bit length, best results are given at appr. 20-40%. For DVIC = 27 MHz the recommended value is $0E_{16}$ for the bit length and 05_{16} for the sample pulse.



If all sync bits of the D-VITC are in the right position of the internal register and the CRC check is o.k. and the 90 bit frame is given, the interrupt flag bit will be set. The D-VITC is stored and readable by CPU until the interrupt flag is cleared.

D-VITC Generator

D-VITC code is generated from data in the D-VITC generator buffer and output during the selected lines. It is possible to select one line, two lines, a block of lines or – for test purposes – all lines of the vertical interval. The CRC and synchronizing bits are automatically generated by the D-VITC generator, but all of the data fields are sent directly from the time and user registers with no modification.

Alternatively there is a settable frame counter to generate up-counting D-VITC automatically. In this mode, even the field flag can be generated. The count mode can be 25-frame, 30-frame drop or 30-frame non-drop. Status bits (except the drop frame bit, which is automatically set, and, if selected, the field bit) and user group data are still taken from the time and user registers. To use the frame counter it has to be enabled and started by storing the desired start time to the time register and writing any value to the counter set register.

The horizontal timing of the generated D-VITC is programmable by the D-VITC start register. However, to meet the ANSI/SMPTE standard this register has to be set to the fixed value $2D_{16}$.

For special purposes the blanking and data signals of the D-VITC generator are accessible at external pins. With this signals it is possible to insert the generated lines into another video channel, even generating an analogue VITC is possible.

Interrupts

Each interrupt source has an corresponding flag bit in the internal flag register. The flag will force the IRQN output to low level if the corresponding enable bit is set. Possible interrupt sources are D-VITC reader (after reading new values), D-VITC generator (after last selected line), V-pulse (start of vertical blanking) , V1-pulse (start of odd field) and V2-pulse (start of even field). V, V1 and V2 pulse interrupt are derived from internal vertical blanking signal (V).

CPU Interface

AV-DVITC is designed to interface to 8-bit microprocessors with multiplexed or non-multiplexed data and address busses. The mode is selected by the CSEL signal. In multiplexed mode, ALE signal (address latch enable) is used to store the register address to an internal address register. In non-multiplexed mode, the microprocessor has to select the register address via the address pins. In any case, read cycles are controlled by a negative pulse at RDN and write cycles by a negative pulse at WRN signals.

The address range is 256 (100_{16}) bytes. Actually only at a small amount of these addresses are used for internal registers, but it is not possible to overlay an unused address range with other functions e.g. by a port chip. If the address range of the CPU is small as e.g. the Z80 I/O or paged memory access of 8051, the CSN signal has to be used to avoid read or write access to undefined register address of the AV-DVITC.

Low-cost Chip Versions

There are three low-cost versions of the AV-DVITC: AV-DVITCB, AV-DVITCR and AV-DVITCG. The only difference to the AV-DVITC (apart from the price) is that the AV-DVITCB is a D-VITC reader/generator but with no frame counter, the AV-DVITCR is a D-VITC reader (it has no D-VITC generator) and the AV-DVITCG is a D-VITC generator (it has no frame counter and no D-VITC reader). All other components like CPU interface, video channel etc. are identical to the original AV-DVITC.

Pin Function Table

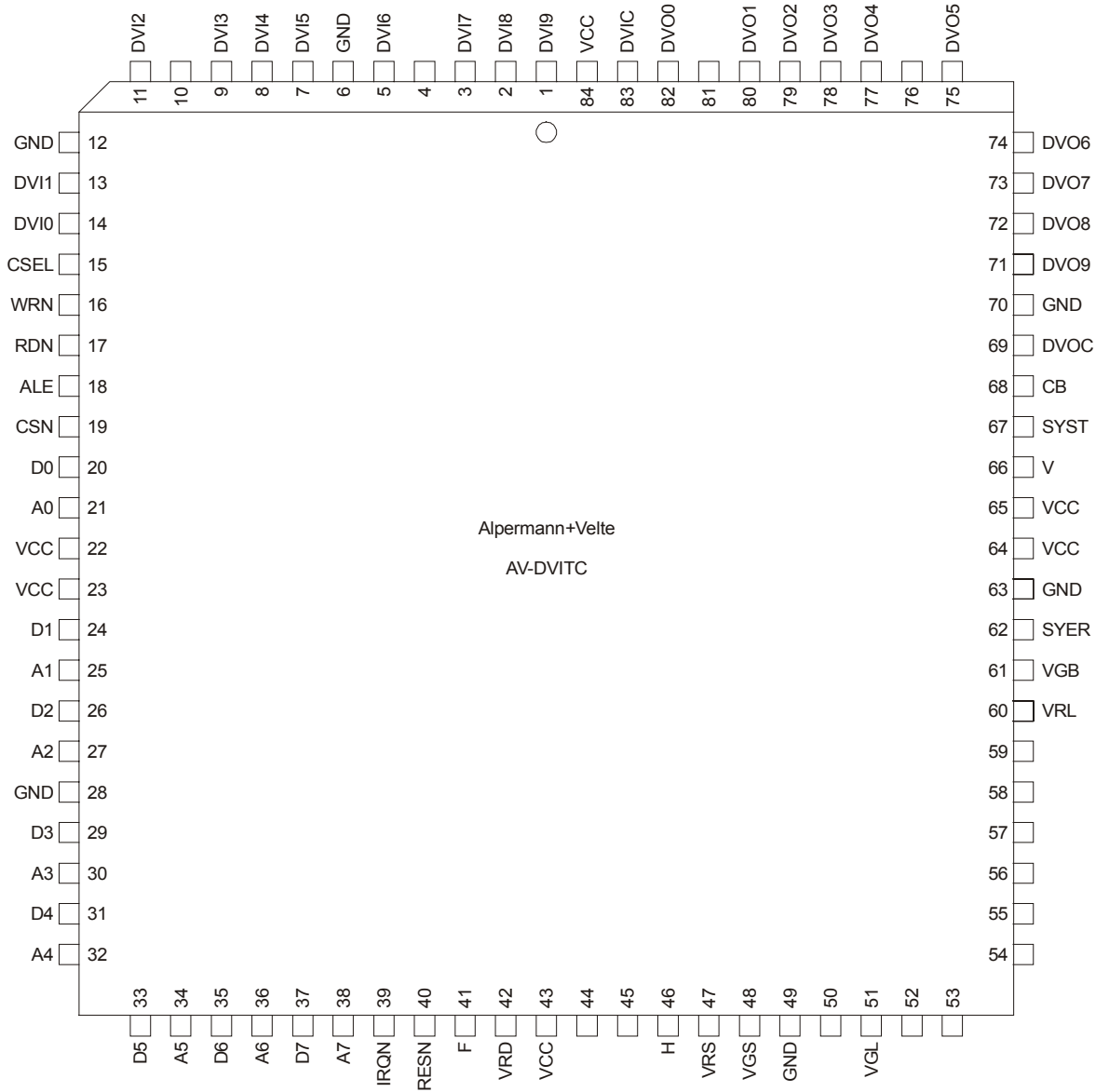
Pin No.	Pin Name	I/O	Description
1	DVI9	I	Video input bit 9
2	DVI8	I	Video input bit 8
3	DVI7	I	Video input bit 7
5	DVI6	I	Video input bit 6
6	GND	I	Logic ground
7	DVI5	I	Video input bit 5
8	DVI4	I	Video input bit 4
9	DVI3	I	Video input bit 3
11	DVI2	I	Video input bit 2
12	GND	I	Logic ground
13	DVI1	I	Video input bit 1
14	DVI0	I	Video input bit 0
15	CSEL	I	CPU bus select
16	WRN	I	Write pulse
17	RDN	I	Read pulse
18	ALE	I	Address latch enable
19	CSN	I	Chip select
20	D0	I/O	Data bus bit 0
21	A0	I	Address bit 0
22	VCC	I	Power supply
23	VCC	I	Power supply
24	D1	I/O	Data bus bit 1
25	A1	I	Address bit 1
26	D2	I/O	Data bus bit 2
27	A2	I	Address bit 2
28	GND	I	Logic ground
29	D3	I/O	Data bus bit 3
30	A3	I	Address bit 3
31	D4	I/O	Data bus bit 4
32	A4	I	Address bit 4
33	D5	I/O	Data bus bit 5
34	A5	I	Address bit 5
35	D6	I/O	Data bus bit 6
36	A6	I	Address bit 6
37	D7	I/O	Data bus bit 7

Pin No.	Pin Name	I/O	Description
38	A7	I	Address bit 7
39	IRQN	OD ¹	Interrupt request
40	RESN	I	System reset
41	F	O	Field-pulse
42	VRD	I	External D-VITC input
43	VCC	I	Power supply
46	H	O	H-pulse
47	VRS	O	Extracted D-VITC
48	VGS	O	D-VITC gen. signal
49	GND	I	Logic ground
51	VGL	O	D-VITC gen. lines
60	VRL	O	D-VITC reader lines
61	VGB	O	D-VITC gen. blanking
62	SYER	O	Sync Error
63	GND	I	Logic ground
64	VCC	I	Power supply
65	VCC	I	Power supply
66	V	O	V-pulse
67	SYST	O	Sync Start
68	CB	O	Phase CB
69	DVOC	O	Video output clock
70	GND	I	Power supply
71	DVO9	O	Video output bit 9
72	DVO8	O	Video output bit 8
73	DVO7	O	Video output bit 7
74	DVO6	O	Video output bit 6
75	DVO5	O	Video output bit 5
77	DVO4	O	Video output bit 4
78	DVO3	O	Video output bit 3
79	DVO2	O	Video output bit 2
80	DVO1	O	Video output bit 1
82	DVO0	O	Video output bit 0
83	DVIC	I	Video input clock
84	VCC	I	Power supply

All unassigned pins are defined as outputs and have to be left open.

¹ OD = Open Drain

Pin Diagram



All unassigned pins are defined as outputs and have to be left open.

Signal Description

Pin Name	Description
RESN	System reset. L-level sets all internal registers to 0.
DVI9:0	Parallel video input. DVI9 is the MSB, DVI0 is the LSB in 10-bit mode, but DVI2 in 8-bit mode.
DVIC	Video input clock. Used to clock the Parallel video input data through the internal processing stages. The frequency is 27 MHz typically.
DVO9:0	Parallel video output. DVO9 is the MSB, DVO0 is the LSB in 10-bit mode, but DVO2 in 8-bit mode.
DVOC	Video output clock. Used to clock the Parallel video output data to the next chip, e.g. a parallel to serial encoder.
CSEL	CPU bus select. Set to H-level for multiplexed mode and L-level for non-multiplexed mode of data and address busses.
ALE	Address latch enable. Used to latch the address of the internal registers from the data bus to the internal address register. Only used in multiplexed mode (CSEL = H)
D7:0	Data bus. Used to transfer data from the internal registers to the microprocessor and vice versa.
A7:0	Address bus. Used to select any of the internal registers. Only used in non-multiplexed mode (CSEL = L)
IRQN	Interrupt request. Forced to L-level if any interrupt condition and the corresponding interrupt enable bit are both true. This is an open drain output, it needs an external pull-up resistor allowing to wired-ANDed to a common level triggered microprocessor interrupt input.
CSN	Chip select. A negative pulse is used to select any of the internal registers. With CSN = H-level the data bus is in high impedance state and no data is transferred to the microprocessor or vice versa.
RDN	Read pulse. A negative pulse is used to transfer data from any internal register to the microprocessor.
WRN	Write pulse. A negative pulse is used to store data from the data bus to any internal register.
H	H-pulse. Positive pulses indicate the horizontal blanking period.
V	V-pulse. Positive pulses indicate the vertical blanking period.
F	Field-pulse. L-level in odd field (V1), H-level in even field (V2).
VRS	Extracted D-VITC. This is the result of the comparison of the video signal with the D-VITC reader threshold.
VRD	External D-VITC input. Use this to get VITC data from external video channel.
VRL	D-VITC reader lines. This is the output of the line selector of the D-VITC reader. The reader accepts data if this signal has H-level.

Pin Name	Description
VGB	D-VITC generator blanking. Active H-level in every line D-VITC has to be generated. With this signal together with VGS signal it is possible to insert D-VITC generator data to an external video channel.
VGS	D-VITC generator signal. Description see VGB above.
VGL	D-VITC generator lines. This is the output of the line selector of the D-VITC generator. The generator is enabled if this signal has H-level.
SYST	Sync Start. H-level if a sync word (3FF - 000) in the video data stream is detected. This might be useful as test signal.
SYER	Sync Error. H-level if the decoding of the sync word results in an error. This might be useful as test signal.
CB	Phase CB. H-level if the CB sample in the video data stream is detected. This might be useful as test signal.

Internal Registers

Addr.	R/W	Name	Data	Description
1F:00		V		Video section
00	R	V_VERSION	D7:0	Version number. Current value is 6C ₁₆ . Will change in future enhanced versions of the chip.
11	W	V_CTRL	D0	0 = Read D-VITC from internal digital video signal 1 = Read D-VITC from pin VRD
			D2	0 = Enable digital output clock DVOC 1 = Set DVOC signal to L-level
12	R	V_SIGNAL	D1	0 = Disable insertion of D-VITC generator 1 = Enable insertion of D-VITC generator
			D2	0 = Enable video channel 1 = Pass through, but keep internal delay
			D3	0 = 10-bit operation of video 1 = 8-bit operation of video by setting pins DVO0 and DVO1 to L-level
			D5	0 = Enable video channel 1 = Pass through, bypass internal delay
15:13		V_IRQR		Reset interrupt flags section
13	W	V_IRQR_VP	any	Reset V-pulse interrupt flag
14	W	V_IRQR_V1	any	Reset V1-pulse interrupt flag
15	W	V_IRQR_V2	any	Reset V2-pulse interrupt flag
17	W	V_IRQE	D0	1 = Enable D-VITC reader interrupt
			D1	1 = Enable D-VITC generator interrupt
			D2	1 = Enable V-pulse interrupt
			D3	1 = Enable V1-pulse interrupt
			D4	1 = Enable V2-pulse interrupt
17	R	V_IRQF	D0	D-VITC reader interrupt flag
			D1	D-VITC generator interrupt flag
			D2	V-pulse interrupt flag
			D3	V1-pulse interrupt flag
			D4	V2-pulse interrupt flag
1B:18		V_COUNT		Read frame counter section
18	R	V_COUNT_F	D3:0	Units of frames
			D5:4	Tens of frames
19	R	V_COUNT_S	D3:0	Units of seconds
			D6:4	Tens of seconds
1A	R	V_COUNT_M	D3:0	Units of minutes
			D6:4	Tens of minutes
1B	R	V_COUNT_H	D3:0	Units of hours
			D5:4	Tens of hours

Addr.	R/W	Name	Data	Description
2F:20		R		D-VITC reader section
27:20		R_VITC		D-VITC reader time and user code section
20	R	R_VITC_F	D3:0	Units of frames
			D5:4	Tens of frames
			D6	D-VITC status bit 14 ¹
			D7	D-VITC color frame flag
21	R	R_VITC_S	D3:0	Units of seconds
			D6:4	Tens of seconds
			D7	D-VITC status bit 35 ²
22	R	R_VITC_M	D3:0	Units of minutes
			D6:4	Tens of minutes
			D7	D-VITC status bit 55 ³
23	R	R_VITC_H	D3:0	Units of hours
			D5:4	Tens of hours
			D6	D-VITC binary group flag 1 (BGF1)
			D7	D-VITC status bit 75 ⁴
24	R	R_VITC_12	D3:0	1 st binary group
			D7:4	2 nd binary group
25	R	R_VITC_34	D3:0	3 rd binary group
			D7:4	4 th binary group
26	R	R_VITC_56	D3:0	5 th binary group
			D7:4	6 th binary group
27	R	R_VITC_78	D3:0	7 th binary group
			D7:4	8 th binary group
28	W	R_THRS	D7:0	Threshold. Nominal value is 68 ₁₆ .
29	W	R_WIDTH	D4:0	Data bit width. Nominal value is 0E ₁₆ .
2A	W	R_LINE1	D4:0	Line select 1. There is a one-line offset in line counting. E.g. to select line 14, write 15 to this register.
2B	W	R_LINE2	D4:0	Line select 2. See description of R_LINE1 above.
2C	W	R_SAMPLE	D4:0	Data bit sample pulse. Nom. value is 05 ₁₆ .
2D	W	R_CTRL	D1:0	Line select mode: 00 = Two lines 01 = Block of lines 11 = All lines To select only one line, set to "two lines" and set R_LINE1 = R_LINE2.
2E	W	R_IRQR	any	Reset D-VITC reader interrupt flag

¹ D-VITC status bit 14: 30-frame: Drop frame flag, 25-frame: Unassigned

² D-VITC status bit 35: 30-frame: Field flag, 25-frame: Binary Group Flag 0 (BGF0)

³ D-VITC status bit 55: 30-frame: Binary Group Flag 0 (BGF0), 25-frame: Binary Group Flag 2 (BGF2)

⁴ D-VITC Status Bit 75: 30-frame: Binary Group Flag 2 (BGF2), 25-frame: Field Flag

Data Sheet AV-DVITC

Addr.	R/W	Name	Data	Description
3F:30		G		D-VITC generator section
37:30		G_VITC		D-VITC generator time and user code sect.
30	W	G_VITC_F	D3:0	Units of frames
			D5:4	Tens of frames
			D6	D-VITC status bit 14 ¹
			D7	D-VITC color frame flag
31	W	G_VITC_S	D3:0	Units of seconds
			D6:4	Tens of seconds
			D7	D-VITC status bit 35 ²
32	W	G_VITC_M	D3:0	Units of minutes
			D6:4	Tens of minutes
			D7	D-VITC status bit 55 ³
33	W	G_VITC_H	D3:0	Units of hours
			D5:4	Tens of hours
			D6	D-VITC binary group flag 1 (BGF1)
			D7	D-VITC status bit 75 ⁴
34	W	G_VITC_12	D3:0	1 st binary group
			D7:4	2 nd binary group
35	W	G_VITC_34	D3:0	3 rd binary group
			D7:4	4 th binary group
36	W	G_VITC_56	D3:0	5 th binary group
			D7:4	6 th binary group
37	W	G_VITC_78	D3:0	7 th binary group
			D7:4	8 th binary group

¹ D-VITC status bit 14: 30-frame: Drop frame flag, 25-frame: Unassigned

² D-VITC status bit 35: 30-frame: Field flag, 25-frame: Binary Group Flag 0 (BGF0)

³ D-VITC status bit 55: 30-frame: Binary Group Flag 0 (BGF0), 25-frame: Binary Group Flag 2 (BGF2)

⁴ D-VITC Status Bit 75: 30-frame: Binary Group Flag 2 (BGF2), 25-frame: Field Flag

Addr.	R/W	Name	Data	Description
38	W	G_LINE1	D4:0	Line select 1. See description of R_LINE1 above.
39	W	G_LINE2	D4:0	Line select 2. See description of R_LINE1 above. Write $1F_{16}$ to this register to select the last line of the field.
3A	W	G_CTRL	D1:0	Line select mode: 00 = Two lines 01 = One line 11 = Block of lines
			D2	0 = Enable D-VITC output 1 = Inhibit D-VITC output
			D3	0 = Disable frame counter: Get both D-VITC time and user data from G_VITC registers 1 = Enable frame counter: Get D-VITC time data from frame counter but user data still from G_VITC registers. In 30-frame modes (see D5:4 below) drop flag is set automatically.
			D5:4	Frame counter mode: 00 = 25-frame 10 = 30-frame non-drop 11 = 30-frame drop
			D7	1 = Automatically set field bit of D-VITC data if D3 = 1
3B	W	G_START	D5:0	Horizontal start of D-VITC output within the video line – set to $2B_{16}$ to generate standard D-VITC
3C	W	G_SET	any	Set frame counter from G_VITC time registers
3D	W	G_IRQR	any	Reset D-VITC generator interrupt flag

Notes:

All unused bits of any write register are reserved. Set to 0 to allow future enhancements.

Unused bits of any read register are undefined.

Avoid read or write access to unused registers in the whole address range $00_{16} - FF_{16}$.

Electrical Characteristics

Absolute Maximum Ratings¹

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_I	Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IO}	I/O Sink/Source Current ²	± 20	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Recommended Operating Conditions

Parameter	Min.	Max.	Units
Temperature Range ³	0	+70	°C
Power Supply V_{CC}	4.75	5.25	V

Electrical Specifications

Symbol	Parameter	Min.	Max.	Units
V_{OH} ⁴	$(I_{OH} = -10mA)$ ⁵	2.4		V
	$(I_{OH} = -6mA)$	3.84		V
V_{OL} ⁴	$(I_{OL} = 10mA)$ ⁵		0.5	V
	$(I_{OL} = 6mA)$		0.33	V
V_{IL}		-0.3	0.8	V
V_{IH}		2.0	$V_{CC} + 0.3$	V
Input Transition Time t_R, t_F ⁵			500	ns
C_{IO} I/O Capacitance ^{5,6}			10	pF
Standby Current, I_{CC} ⁷			3	mA
Leakage Current ⁸		-10	10	μA

¹ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommend Operating Conditions.

² Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than $V_{CC} + 0.5V$ or less than GND -0.5V, the internal protection diode will be forwarded biased and can draw excessive current.

³ Ambient temperature (T_A).

⁴ Only one output tested at a time. $V_{CC} = \min$.

⁵ Not tested, for information only.

⁶ $V_{OUT} = 0V, f = 1MHz$.

⁷ Typical standby current = 1mA. All outputs unloaded. All inputs = V_{CC} or GND.

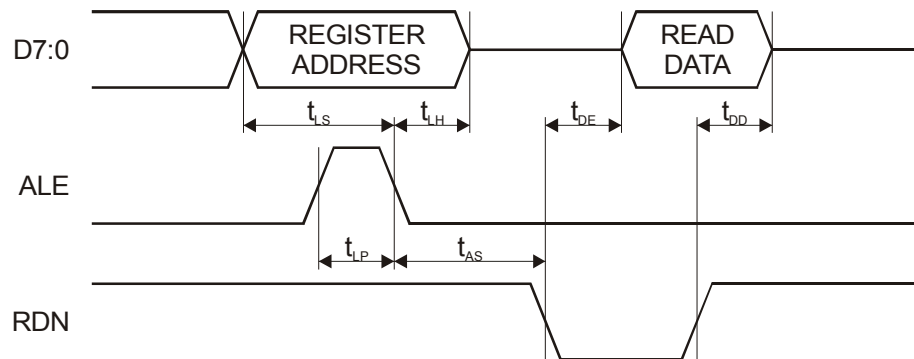
⁸ $V_O, V_I = V_{CC}$ or GND.

Switching Characteristics

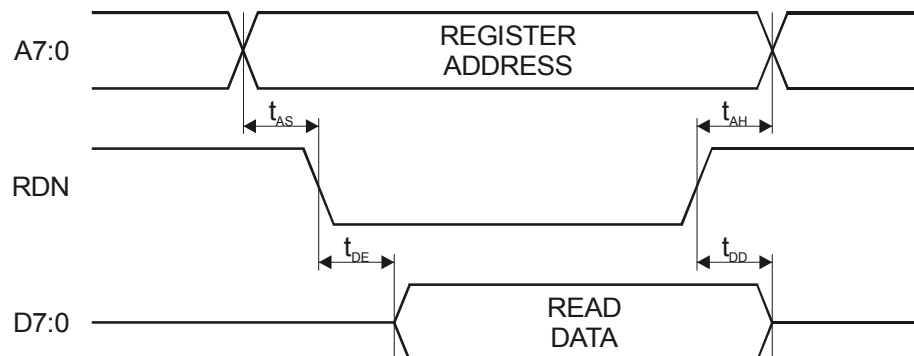
Symbol	Parameter	Min.	Typ.	Max.	Units
t_{LS}	Address Latch Setup Time	50			ns
t_{LP}	Address Latch Pulse Width	50			ns
t_{LH}	Address Latch Hold Time	30			ns
t_{AS}	Address Bus Setup Time	50			ns
t_{AH}	Address Bus Hold Time	30			ns
t_{DS}	Data Bus Setup Time	50			ns
t_{WP}	Write Pulse Width	50			ns
t_{DH}	Data Bus Hold Time	30			ns
t_{DE}	Data Bus Enable Time			50	ns
t_{DD}	Data Bus Disable Time	10			ns
t_{DIC}	Digital Input Clock Cycle Time	35	37		ns
t_{DIS}	Digital Input Data Setup Time	3			ns
t_{DIH}	Digital Input Data Hold Time	3			ns
t_{DOC}	Digital Output Clock Cycle Time		37		ns
t_{DOS}	Digital Output Data Setup Time	10			ns
t_{DOH}	Digital Output Data Hold Time	10			ns

CPU Read Timing

Multiplexed Mode (CSEL = H)

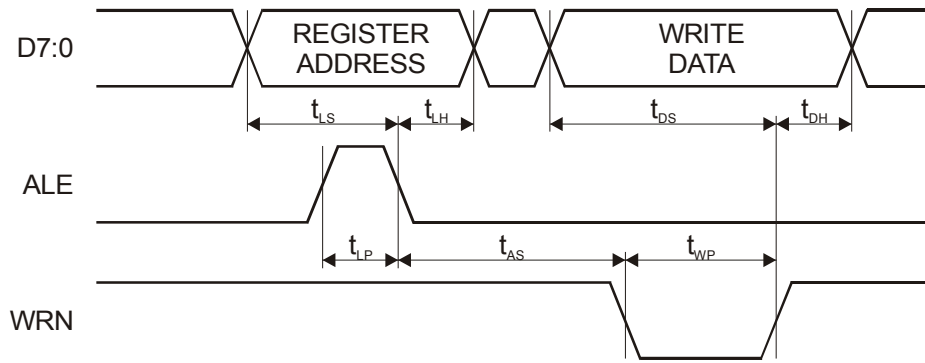


Non-Multiplexed Mode (CSEL = L)

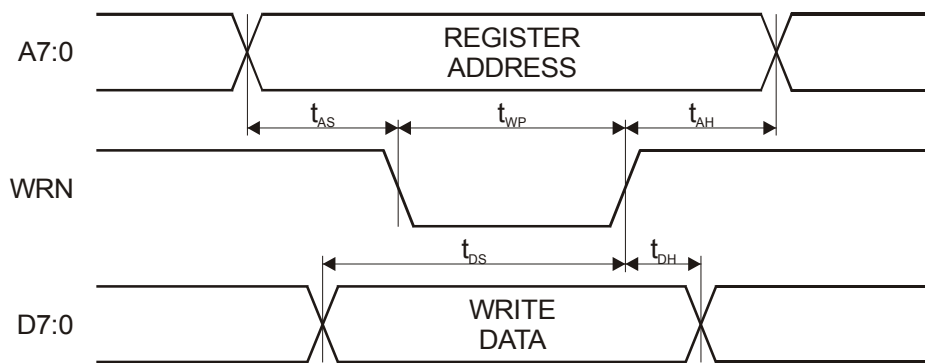


CPU Write Timing

Multiplexed Mode (CSEL = H)

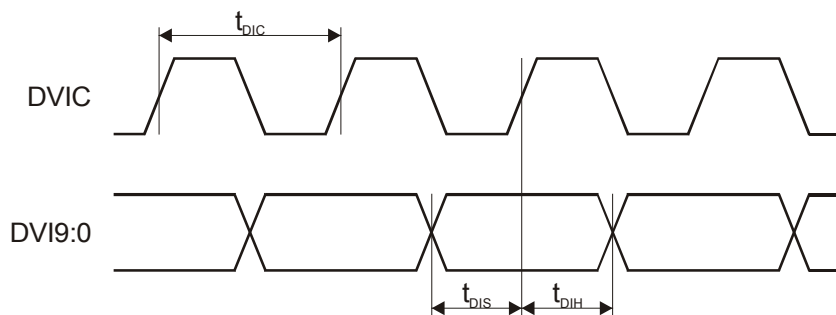


Non-Multiplexed Mode (CSEL = L)

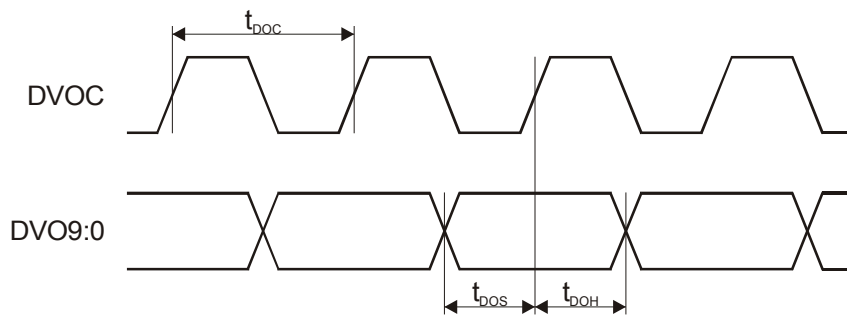


Digital Video

Parallel Input



Parallel Output

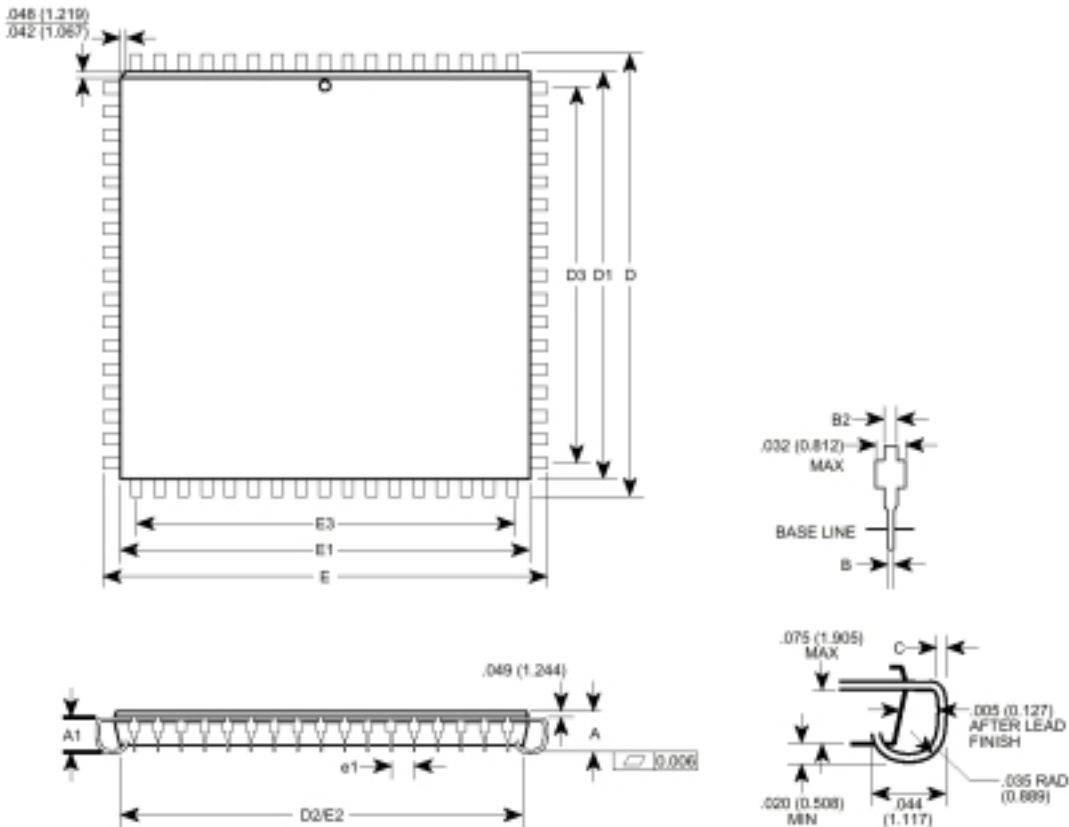


Physical Dimensions

Plastic Leaded Chip Carrier Package, 84 pins (PLCC 84)
JEDEC Equivalent: MS007 AB VAR

Symbol	Min.	Max.
A	0.155 (3.937)	0.175 (4.445)
A1	0.090 (2.286)	0.130 (3.302)
B	0.013 (0.330)	0.027 (0.686)
B2	0.026 (0.660)	0.032 (0.813)
C	0.005 (0.127)	0.011 (0.279)
D/E	1.170 (29.72)	1.210 (30.73)
D1/E1	1.140 (28.96)	1.160 (29.46)
D2/E2	1.090 (27.69)	1.130 (28.70)
D3/E3	1.00 (25.40) nominal	
e1	0.050 (1.270) BSC ¹	

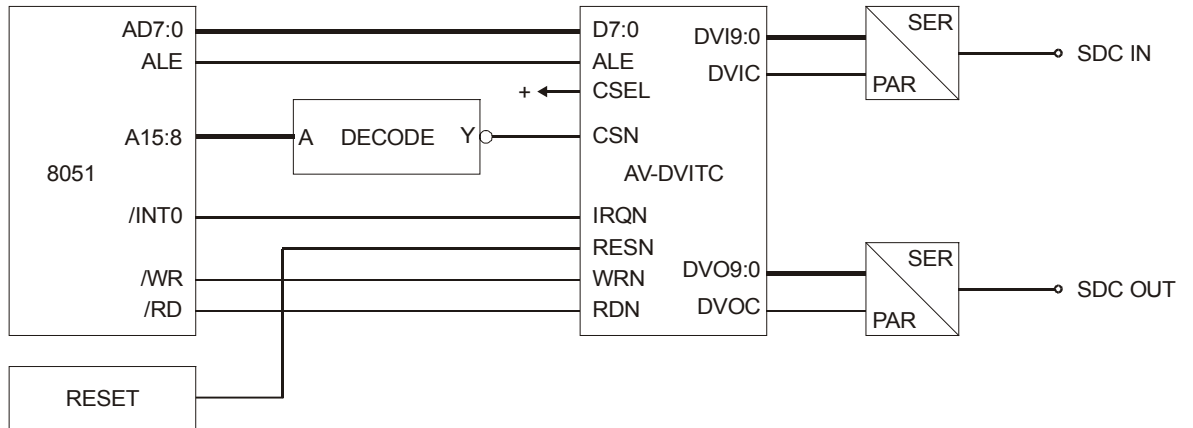
All dimensions are in inches (millimeters).



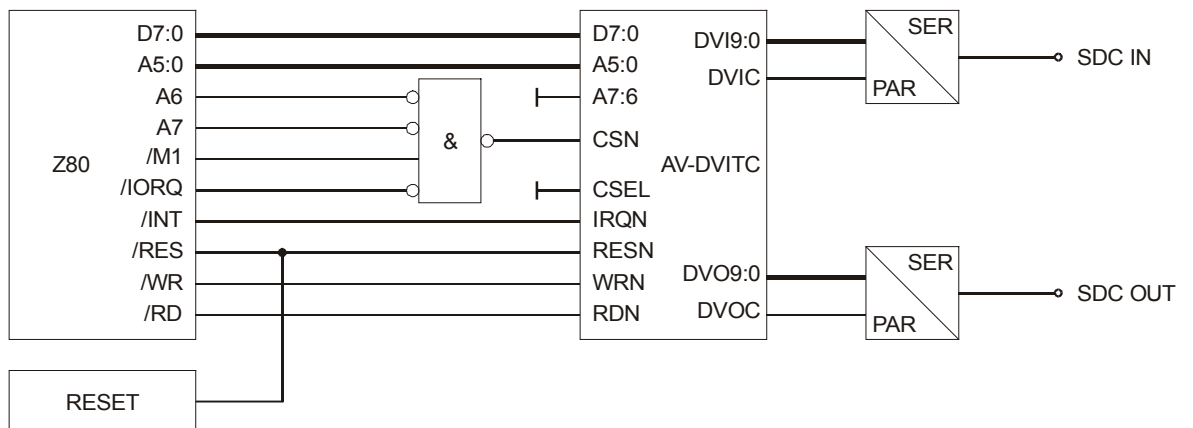
¹ BSC – Basic Space between Centers

Applications

Interface to 8051 MCU



Interface to Z80 CPU



Interface to 68HC11 MCU

